AN-541
Application Note

MEDIUM SCALE INTEGRATION IN THE NUMERICAL CONTROL FIELD

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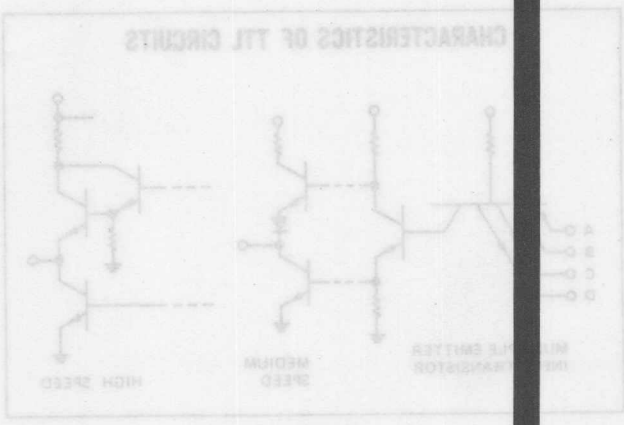
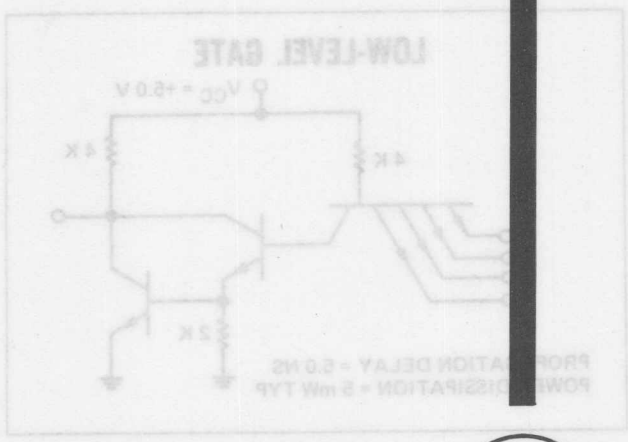
Applications Engineering





Since medium scale integration means complex functions, the logic design engineer must understand both the product and its end use in order that his design be optimized. Transistor-Transistor Logic has a number of devices such as programmable counters, phase detectors, voltage controlled multivibrators, comparators, etc., which are available today in integrated circuit form. The devices can be applied to the numerical controls field and are the subject of this paper.

MOTOROLA *Semiconductor Products Inc.*

MEDIUM SCALE INTEGRATION IN THE NUMERICAL CONTROL FIELD

INTRODUCTION

A number of integrated circuits of medium scale integration complexity are available for use in the numerical control industry. The majority of these devices use the familiar transistor-transistor logic (TTL) configuration as the basic gating configuration for system design. Figure 1 shows the characteristics of a TTL circuit, a multiple emitter input transistor, followed by a phase splitting transistor and an output circuit whose configuration depends on whether it is a medium- or high-speed circuit. For use in medium scale integration, more commonly known as complex functions, Motorola uses a configuration that employs two forms of TTL gates. Shown in Figure 2 is the low-level gate used within the device itself to drive the internal circuitry not requiring high fanout capabilities. The high-level gate in Figure 3 is used to drive loads on the output pins. The following devices will be discussed in detail, and then their applications to various systems will be presented

MC4016	Decade Programmable Counter
MC4018	Binary Programmable Counter
MC4024	Voltage Controlled Multivibrator
MC4044	Frequency/Phase Detector

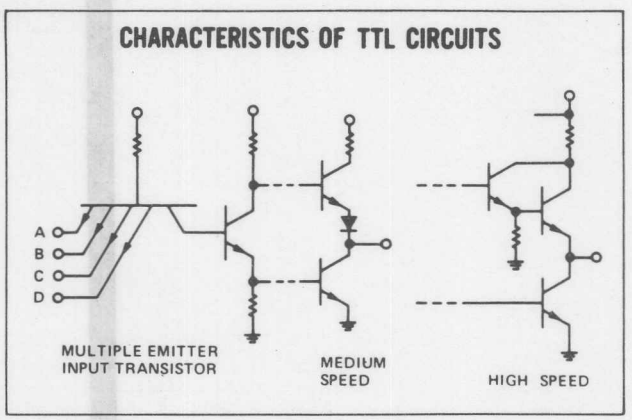


FIGURE 1

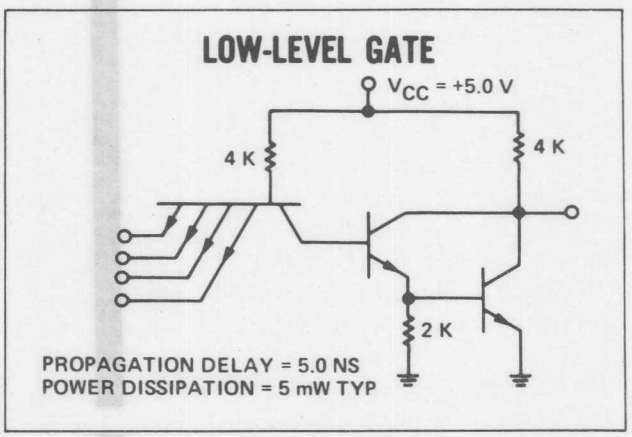


FIGURE 2

MC4016 – DECADE PROGRAMMABLE CASCADEABLE COUNTER

For a single decade counter the clock and gate (G) inputs are normally tied together. When counters are cascaded,

all gate inputs are tied to the original input clock. For purposes of explanation we will consider a single decade counter with the clock and gate tied together. The following explanation refers to Figure 4.

The number to be divided by is placed on inputs P1, P2, P4 and P8 in decade form and $\overline{Pn}$ is set high. When $\overline{Pn}$ is momentarily taken low, the reset/preset logic is enabled and the number appearing on the inputs is preset on the outputs Q1, Q2, Q4 and Q8. Once the desired number has been preset, clocking is initiated and the counter counts down from the preset number. When the counter reaches zero (0000) the Buss (B) output goes high and is fed back to the preset circuit. When the feedback is applied to the preset control, the input number is entered back on the outputs of the counter. This causes the Buss output to return to zero. The resultant output is in the form of a

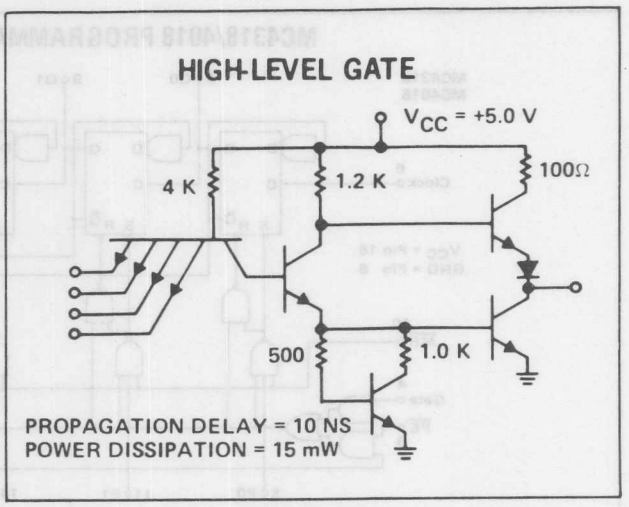
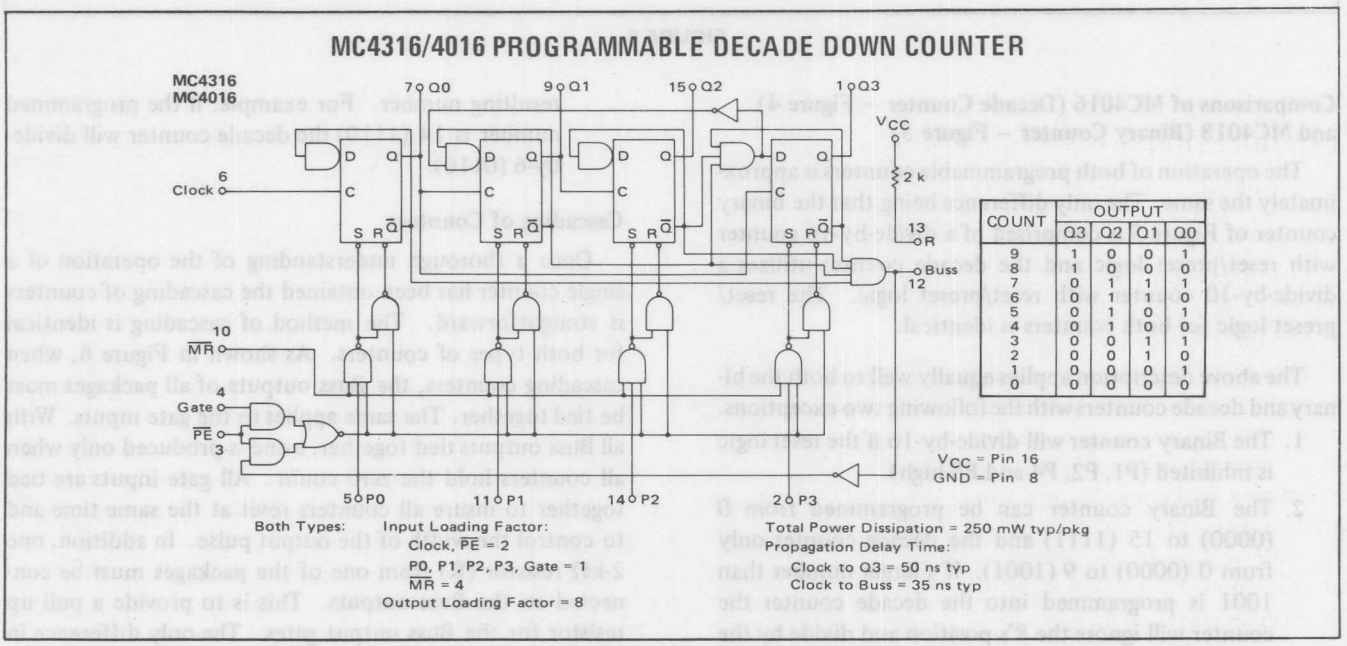


FIGURE 3



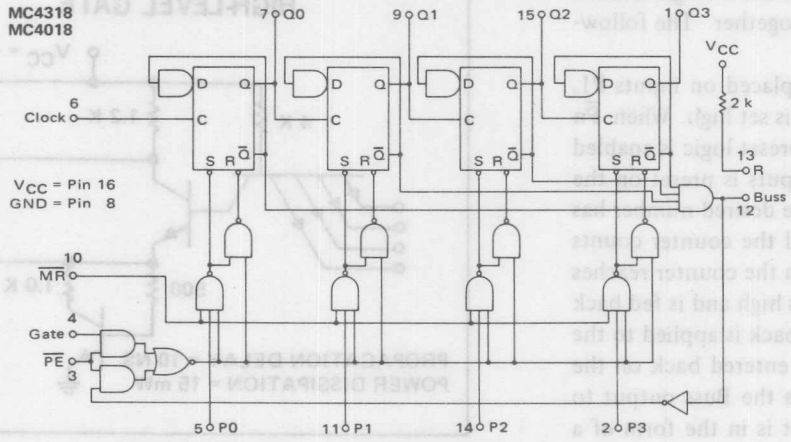
COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

FIGURE 4

pulse. The gate input is to control the pulse width of the Buss output. The Buss output goes to a one when the last clock pulse goes to a one but does not reset the number until the clock goes low. Once the clock goes low both sides of the preset circuit are enabled and the input number can be reset on the outputs of the counter. The pulse from the Buss output is approximately equal to the clock input pulse.

The operation of the decade programmable counter may be further explained by considering an example. Consider the case when it is desired to divide by the number 7 (0111). The number 0111 is placed on inputs P8, P4, P2 and P1 respectively and $\overline{Pn}$ is momentarily taken low. The number 0111 is now on the outputs of the counter. On the first positive transition of the clock the counter goes to 6 (0110). The counter continues to count down on every positive transition of the clock. For the first six clock pulses the Buss output remains low because the count has not reached zero. On the seventh transition the counter goes to 0000 and the Buss output goes high and enables the reset circuit. When the clock goes low the number is again set on the counter outputs and the Buss output goes low. One pulse has now appeared on the Buss output for seven input clock pulses. The counter will continue to divide the clock input by 7 as long as the 7 appears on the inputs. If it is desired to divide by a different number, that number is placed on the appropriate inputs and it will be reset into the counter the next time the counter reaches zero. Since the reset logic is inhibited during normal clocking the new number may be entered while clocking is occurring. If it is desired to enter the new number before the counter reaches zero this can be accomplished by placing the new number on the inputs and taking $\overline{Pn}$ low. The new number will be entered on the outputs and counting will begin from there.

MC4318/4018 PROGRAMMABLE 4-BIT BINARY DOWN COUNTER



COUNT	OUTPUT			
	Q3	Q2	Q1	Q0
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

*L suffix = 16-pin ceramic dual in-line package (Case 620).
P suffix = 16-pin plastic dual in-line package (Case 612).

FIGURE 5

Comparisons of MC4016 (Decade Counter – Figure 4) and MC4018 (Binary Counter – Figure 5)

The operation of both programmable counters is approximately the same. The only difference being that the binary counter of Figure 5 is comprised of a divide-by-16 counter with reset/preset logic and the decade counter utilizes a divide-by-10 counter with reset/preset logic. The reset/preset logic for both counters is identical.

The above description applies equally well to both the binary and decade counters with the following two exceptions.

1. The Binary counter will divide-by-16 if the reset logic is inhibited (P1, P2, P4 and P8 high).
2. The Binary counter can be programmed from 0 (0000) to 15 (1111) and the decade counter only from 0 (0000) to 9 (1001). If a larger number than 1001 is programmed into the decade counter the counter will ignore the 8's position and divide by the resulting number. For example, if the programmed number is 14 (1110) the decade counter will divide-by-6 (0110).

Cascading of Counters

Once a thorough understanding of the operation of a single counter has been obtained the cascading of counters is straightforward. The method of cascading is identical for both types of counters. As shown in Figure 6, when cascading counters, the Buss outputs of all packages must be tied together. The same applies to the gate inputs. With all Buss outputs tied together, a one is produced only when all counters hold the zero count.. All gate inputs are tied together to insure all counters reset at the same time and to control the width of the output pulse. In addition, one 2-kΩ resistor (R) from one of the packages must be connected to the Buss outputs. This is to provide a pull up resistor for the Buss output gates. The only difference in

3 STAGE DECADE PROGRAMMABLE FREQUENCY DIVIDER

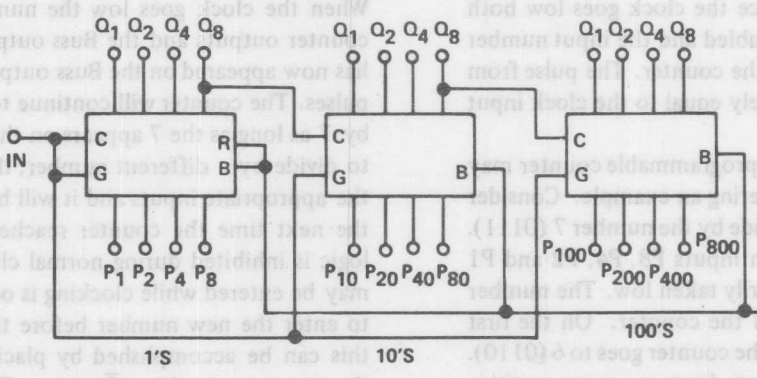


FIGURE 6

the counters being in the method of programming the desired division. The binary counter must be programmed in binary form and the decade in decimal. The reason for the different methods of programming is because of the counting sequence the counters revert to when the reset logic is inhibited. This point will be explained by considering an example for each counter.

Consider the case where decade counters are being used and the desired division is by 325 (0011 0010 0101). The first counter (least significant bit) is programmed to 5 (0101), the second to 2 (0010) and the third (most significant bit) to 3 (0011). After 5 clock pulses the count will be 0000 0010 0011. Since all Buss outputs are ANDed together and 0000 does not exist in the second and third counters, the Buss output remains at zero and the first counter is not reset. The next (sixth) clock pulse produces the count of 1001 0001 0011 or 319. This process continues for 325 pulses until all counters contain 0000. When all counters reach 0000 the Buss outputs go high and the number is reset. One pulse out has been obtained from 325 pulses in. In other words, the clock input has been divided by 325.

For the second case, assume that binary counters are being used and the desired division is again by 325 (0001 0100 0101). The first counter is programmed with 5 (0101), the second to 64 (0100) and the third to 256 (0001). The count proceeds as before for the first five clock pulses. The count is now 0000 0010 1000 reading from least significant to most significant bit. Again the first counter is not reset because all counters do not hold the 0000 count. On the next (sixth) clock pulse the count is 1111 1100 1000 or 319. At this point three things become apparent: 1) the first counter went to a maximum of 1111 instead of 1001 as the decade counters. 2) the outputs are in a straight binary code, and 3) the counters will divide by 16 instead of 10 until they are reset. As before, the Buss output will not go to 1 until there have been 325 clock pulses.

In both cases the results are identical. The only differences occur in the method of coding the input number and the method of counting for the counters.

Because of the difficulty in programming, it is best not to mix types of counters when cascading. An exception to this is when a different counter is used in the most significant position of the cascaded chain. This is true because the most significant counter is always reset when it reaches zero and is never allowed to revert to its natural counting sequence. This feature becomes important in applications where it is desired to divide by numbers in the range of 1000 to 1599. If this is done with all decade counters, four counters would be required. If a binary counter is used in the most significant position only three counters are required (1 binary and 2 decade) without any loss in ease of programming.

MC4324/MC4024 – DUAL VOLTAGE CONTROLLED MULTIVIBRATOR

This circuit consists of two current-mode, emitter-coupled multivibrators, with appropriate level shifting to produce outputs compatible with TTL logic levels. Frequency control is accomplished through the use of voltage-variable current sources that control the voltage charging rate of a single capacitor. The upper operating limit of this VCM is 30 MHz.

Figure 7 shows the schematic of the MC4324/4024. Note that there are multiple B+ and ground connections. This has been done to provide some degree of isolation between units to keep logic current transients out of the oscillator circuit in critical applications. To disable one

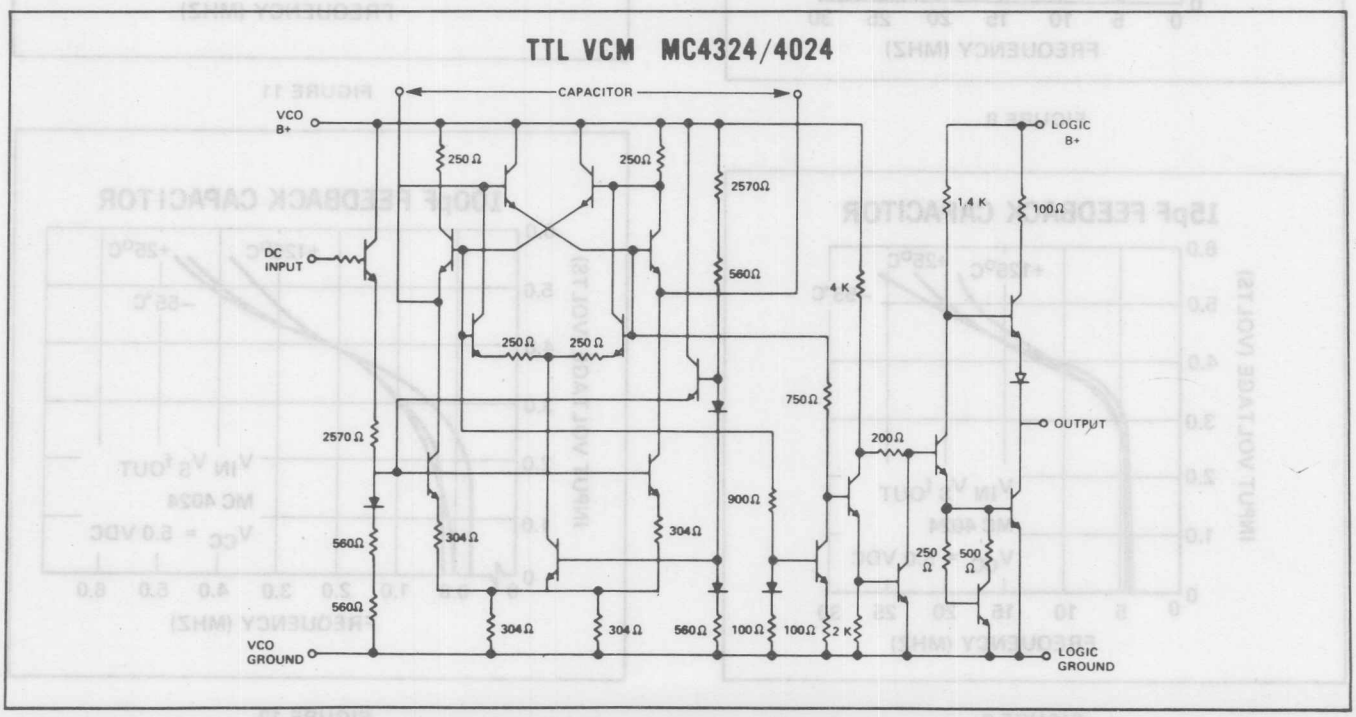


FIGURE 7

VCM, its V_{CC} is disconnected from B+; all grounds must always be connected to insure substrate grounding and good isolation.

The frequency of the voltage controlled oscillator (MC4024) is determined by the external capacitor in the feedback loop. The required value of the capacitor may be determined from either of the following equations.

$$C = \frac{500}{f_{max}} \mu F$$

$$C = \frac{100}{f_{min}} \mu F$$

The frequency of the device is controlled in a nearly linear manner over approximately a 5:1 range by changing the control voltage. The following set of Figures (8 through 13) represent the typical operating characteristics using different values of capacitance in the feedback loop. The curves include room temperature data (25°C) as well as the temperature extremes of -55°C and +125°C.

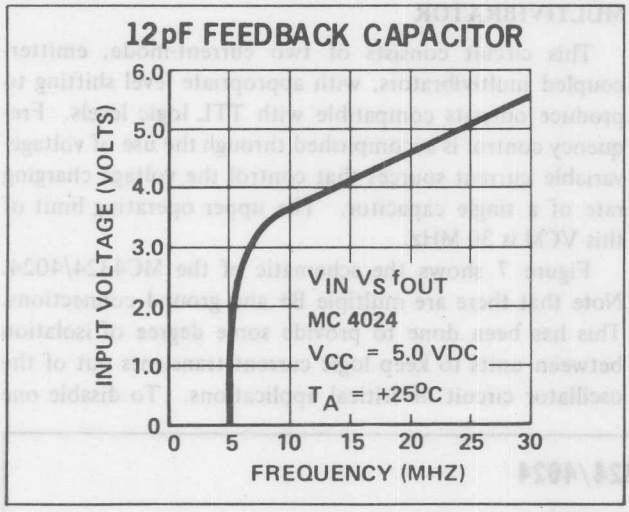


FIGURE 8

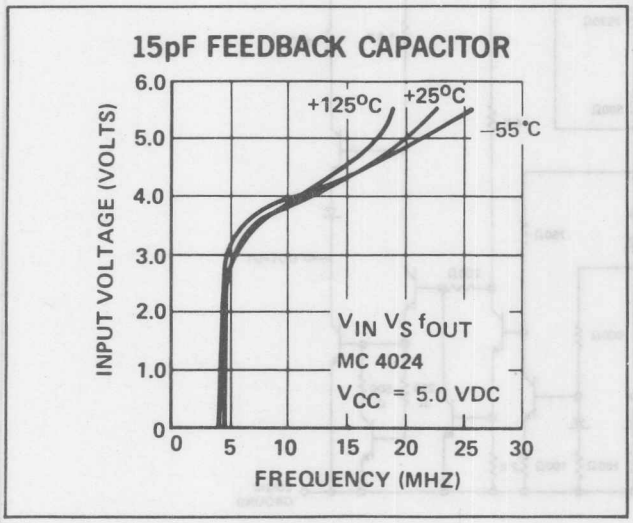


FIGURE 9

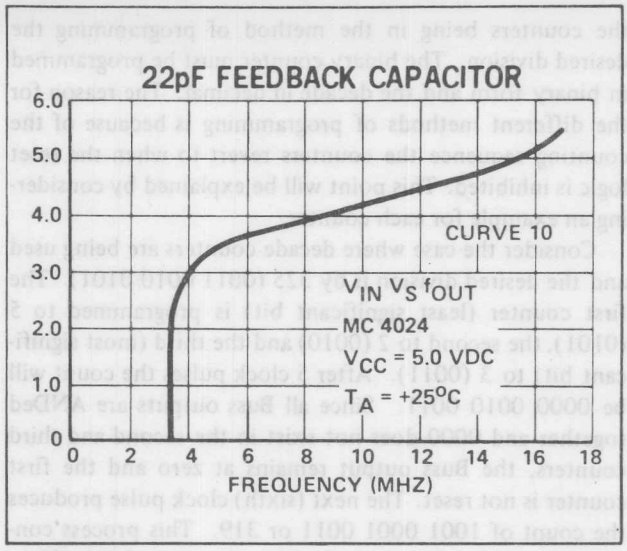


FIGURE 10

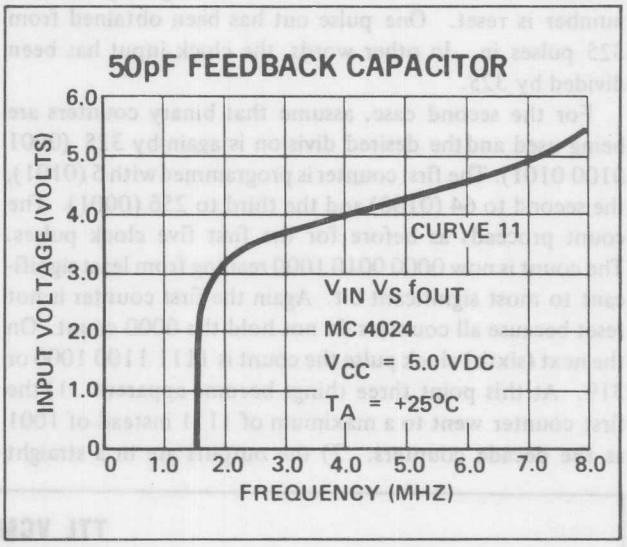


FIGURE 11

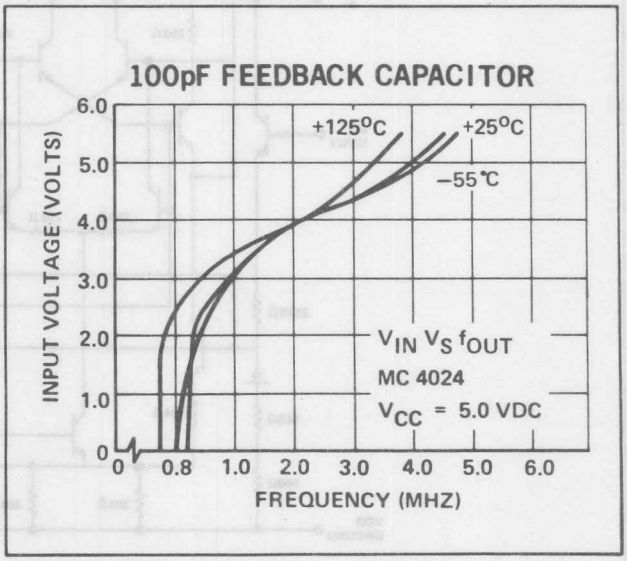


FIGURE 12

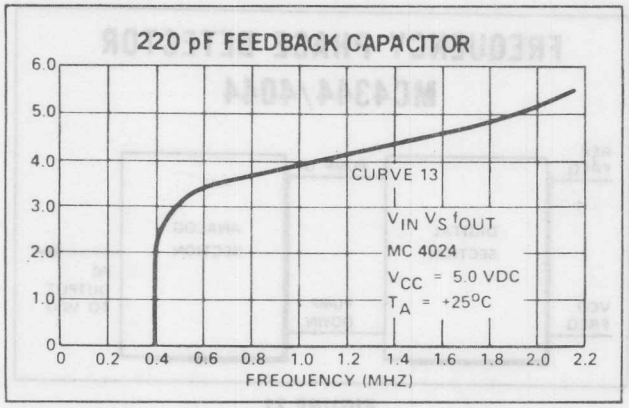


FIGURE 13

Using voltage-variable capacitance diodes in the feedback loop the frequency range of the MC4024 may be increased substantially. The MV1401-03-04-05 hyperabrupt-junction voltage-variable capacitance diodes provide capacitance changes of greater than ten times for a bias change ranging from two-to-ten volts. Figure 14 is the diode capacitance as a function of reverse voltage for these devices.

By using the configuration of Figure 15 the control voltage may be used to bias the voltage variable diodes and change their effective capacitance. The MC1456 is an internally compensated high performance monolithic operational amplifier and is used in the non-inverting feedback mode. Under the conditions shown the gain of the MC1456 is equal to 2. The voltage applied to the MV1403 voltage variable diodes is twice the control voltage V_{in}. Figure 16 relates frequency out, f_o, to voltage in, V_{in}, for Figure 15. Figures 17 and 18 are enlarged portions of Figure 16.

The frequency range of the MC4024 may be decreased by adding resistors from the feedback capacitor terminals to ground. Figure 19 relates frequency out, f_o, to voltage in, V_{in}, using a capacitance of 2000 pF between terminals and two 470 Ω resistors to ground.

MC4344/MC4044 – FREQUENCY/PHASE DETECTOR

Two digital phase detectors and an analog charge pump circuit make up the circuit of Figure 20. The TTL inputs are converted to a dc voltage level for use in frequency discrimination and phase locked loop applications.

The two phase detectors have common inputs. Phase-frequency detector No. 1 is in lock and both outputs are high when the negative transitions of the input (VI) and the reference (RI) are equal in frequency and phase. If VI is lower in frequency or lags in phase, then the U1 output goes low; conversely the D1 output goes low when the VI input is higher in frequency or leads the reference in phase. It is important to note that the duty cycle of the VI input or the RI input is not important since negative transitions control system operation.

Phase detector No. 2 is in lock when the VI input phase lags the reference phase by 90 degrees. In this case, when lock occurs the V2 and D2 outputs go alternately low with equal pulse widths. If the VI input phase lags by more than 90 degrees, U2 will remain low longer than D2. If the VI input phase lags the reference phase by less than 90 degrees,

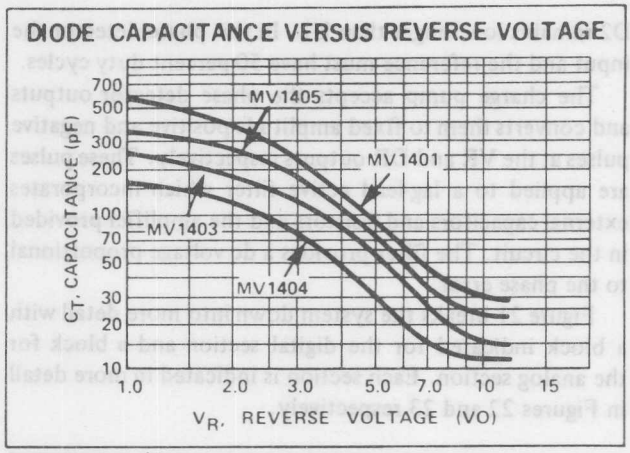


FIGURE 14

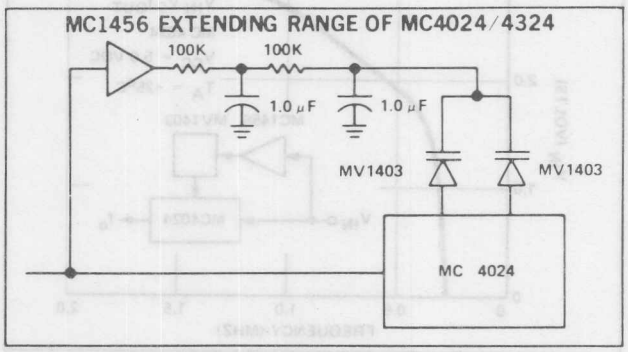


FIGURE 15

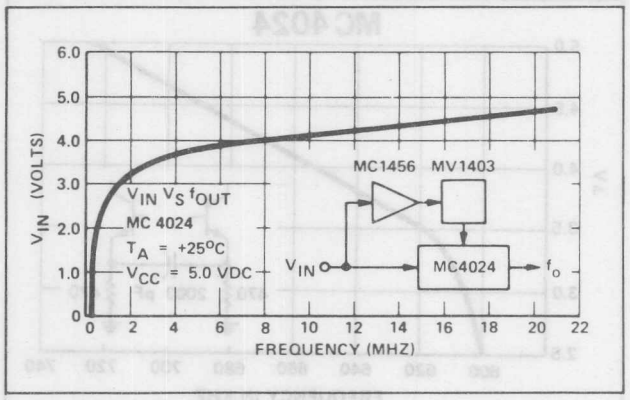


FIGURE 16

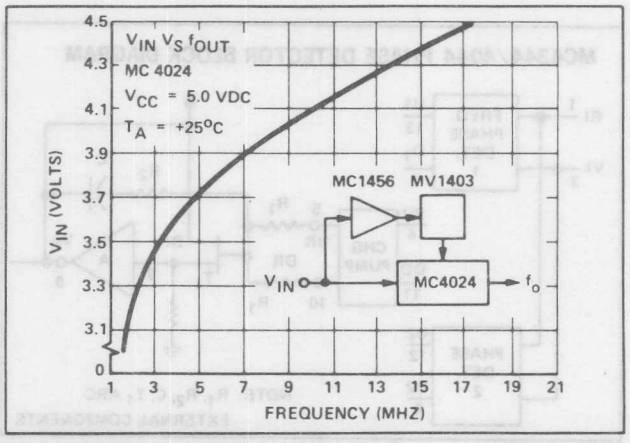


FIGURE 17

D2 remains low longer than U2. In this phase detector the input and the reference must have 50 percent duty cycles.

The charge pump accepts the phase detector outputs and converts them to fixed amplitude positive and negative pulses at the VR and DR outputs respectively. These pulses are applied to a lag-lead active filter which incorporates external capacitors and resistors and the amplifier provided in the circuit. The filter provides a dc voltage proportional to the phase error.

Figure 21 breaks the system down into more detail with a block indicated for the digital section and a block for the analog section. Each section is indicated in more detail in Figures 22 and 23 respectively.

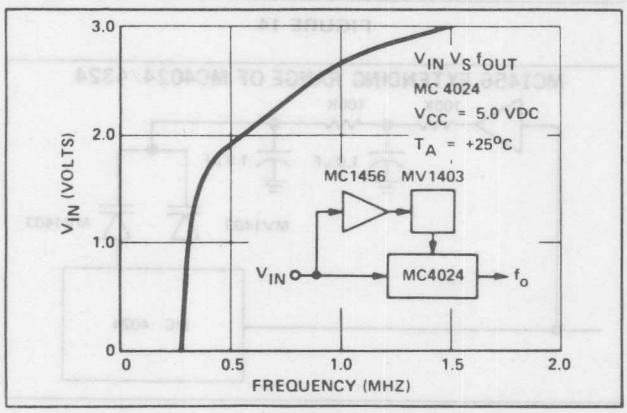


FIGURE 18

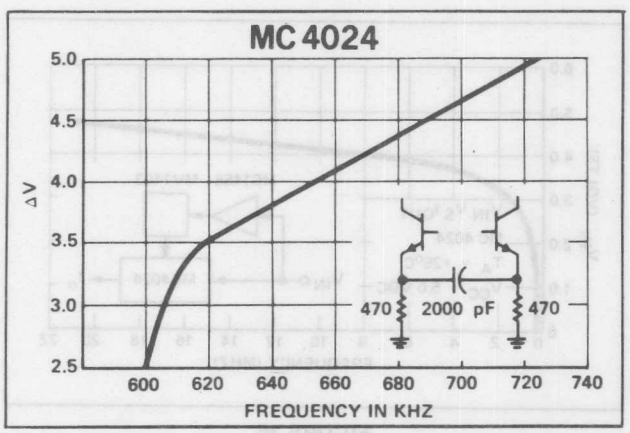


FIGURE 19

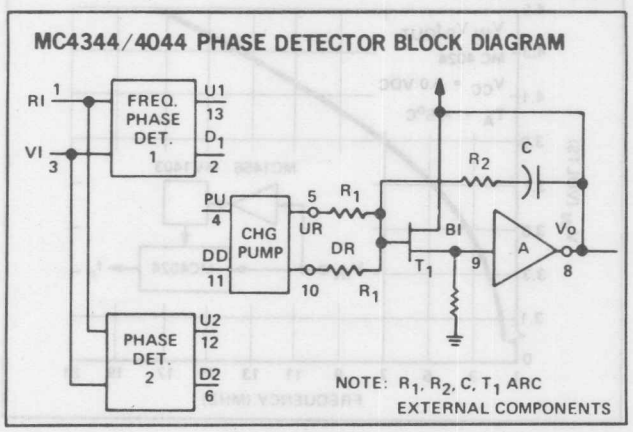


FIGURE 20

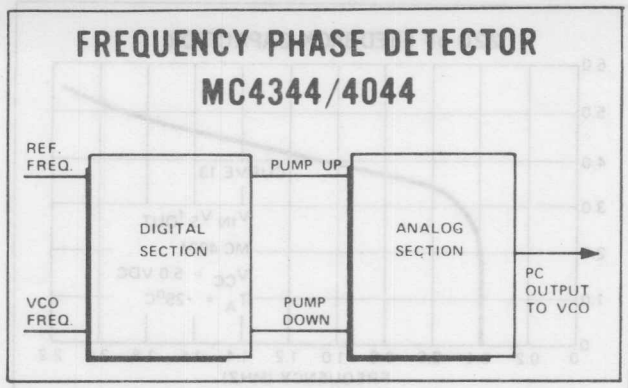


FIGURE 21

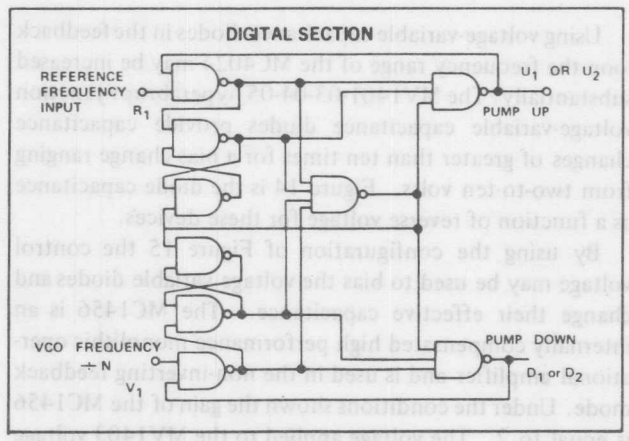


FIGURE 22

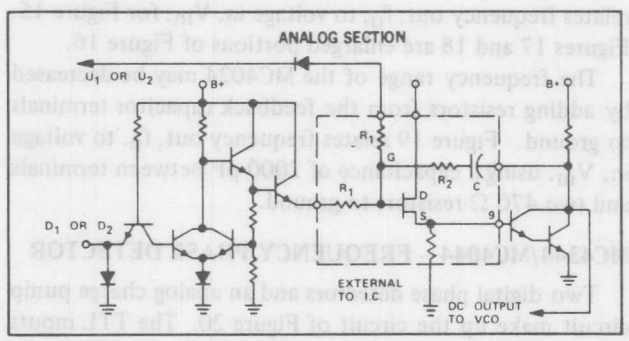


FIGURE 23

APPLICATIONS

Various applications of the previously discussed devices are possible. A number of systems were designed using the MC4024 (Voltage Controlled Multivibrator), the MC4044 (Frequency/Phase Detector) and either the MC4016 (Decade Programmable Down Counter) or the MC4018 (Binary Programmable Down Counter).

Audio Frequency Comparator

A system whereby an unknown frequency is determined by comparing it to a known frequency is shown in Figure 24. The voltage controlled multivibrator, MC4024, is used with a 2 MHz crystal in the feedback loop. Two decade counters (non-programmable) count the frequency down to 20 kHz. Three programmable down counters, MC4016s, provide an output as low in frequency as 20 Hz. One edge

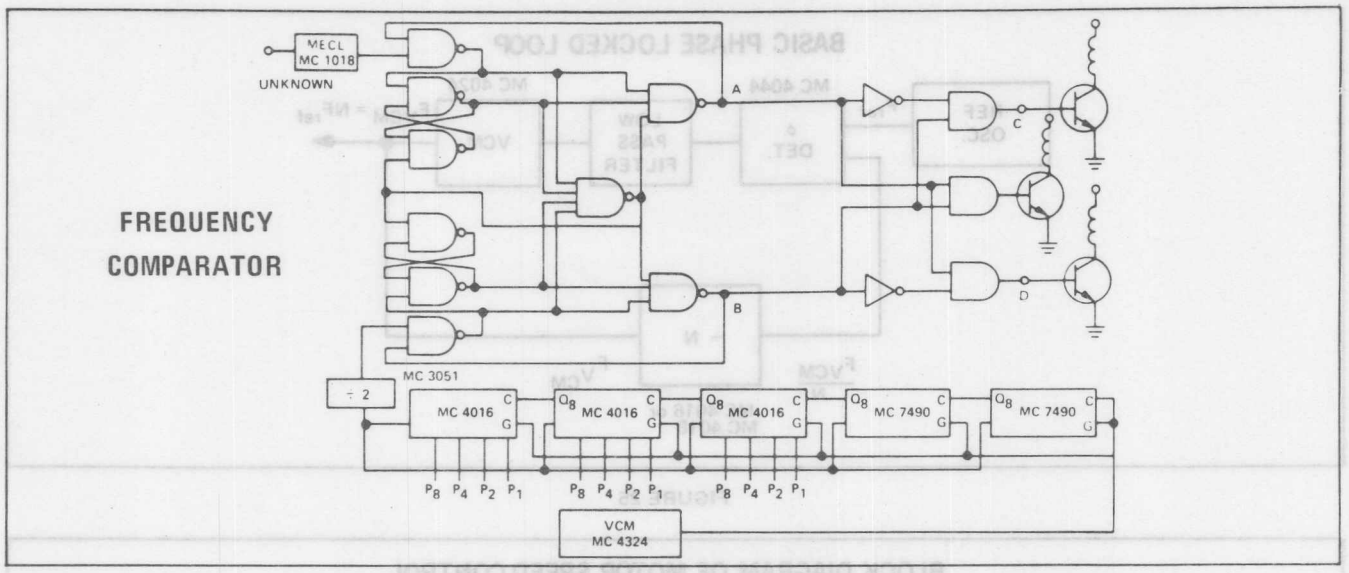


FIGURE 24

trigger flip-flop, MC3051, shapes the output signal of the last programmable counter into a square wave of 50% duty cycle. The unknown signal is fed into a MECL gate, the MC1018 which detects zero crossing of the incoming signal. Using this device the unknown signal may be a sine wave signal and will be converted into a square wave. Both the unknown signal and the reference signal are fed into the digital section of the phase detector. If both signals are the same frequency both points A and B will be at a high level. Outputs C and D will be low and both indicator lights will be off. If the unknown signal is lower in frequency than the reference signal, then point A will go to a low level which in turn will enable the transistor at point C, turning on its indicator light. If the unknown signal is higher in frequency than the reference signal, then point B goes to a low level and the transistor at point D is enabled. The "P" inputs are adjusted for a frequency match—both high indicator and low indicator off – and the unknown frequency determined.

Frequency Synthesizer

The frequency synthesizer loop of Figure 25 achieves a stable state when $F_{VCM} = NF_{ref}$. Until this condition exists, the VCM will continue changing frequency. When the VCM locates the proper frequency the loop locks.

The phase lock loop is used to compare the internally generated frequency of the MC4024 with the external frequency from the reference oscillator and lock the two together. The error voltage that results from comparing the two signals in the digital section of the frequency/phase detector results in a pump-up or pump-down signal to the charge pump, depending on whether the VCM frequency is slower or faster, respectively, than the reference frequency. The charge pump feeds the filter, which determines whether the locking frequency will be underdamped, critically damped, or overdamped. These are a function of the filter elements R1, R2, and C. The filter output feeds the VCM to control its frequency.

Motor Speed Control

Using the previously discussed devices it is possible to provide a motor speed control circuit. Figure 26 is the block diagram of a motor speed control system with the interior phase lock loop shown in more detail in Figure 27. The interior loop accepts the signal from the ac motor pick-up circuit and increases the frequency to the 2 MHz region. The frequency from the interior loop is compared to a reference signal generated from the crystal controlled MC4024 (Voltage Controlled Multivibrator) in conjunction with the MC4018 (Binary Programmable Counter) shown in greater detail in Figure 28. The programmable counter in Figure 28 controls the speed of the ac motor. The ac motor and the entire loop, therefore, respond to the frequency that is programmed on the inputs of the counter. The pick-up circuit of Figure 29 has a phototransistor (MRD310) which picks up a signal from a single strip painted on the shaft of the ac motor. Fiber Optics (not shown on the figure) are used to concentrate the reflection from the shaft and provide the necessary signal to the transistors base. The one-shot multivibrator (MC8601) is necessary to eliminate the effects of shaft jitter which would false trigger the extremely fast response of the MC4044 (Frequency Phase Detector). The ac control circuit which converts the frequency/phase detector output of Figure 28 to a usable signal to control the ac motor is indicated in Figure 30. This circuit utilizes both a bi-lateral switch, and a MAC 2 triac. The conversion of a dc voltage to an ac signal is discussed in more detail in Motorola Application Note AN-482.

CONCLUSION

A number of IC functions of medium scale integrated complexity have been discussed which may be used in the numerical controls field. The application of these devices is not limited to this field but they are usable in various industrial and computer systems. Industrial applications include differential voltmeters, ammeters, counters, etc. Computer applications include system clocks, divide-by-N counters, tape drive controls, etc.

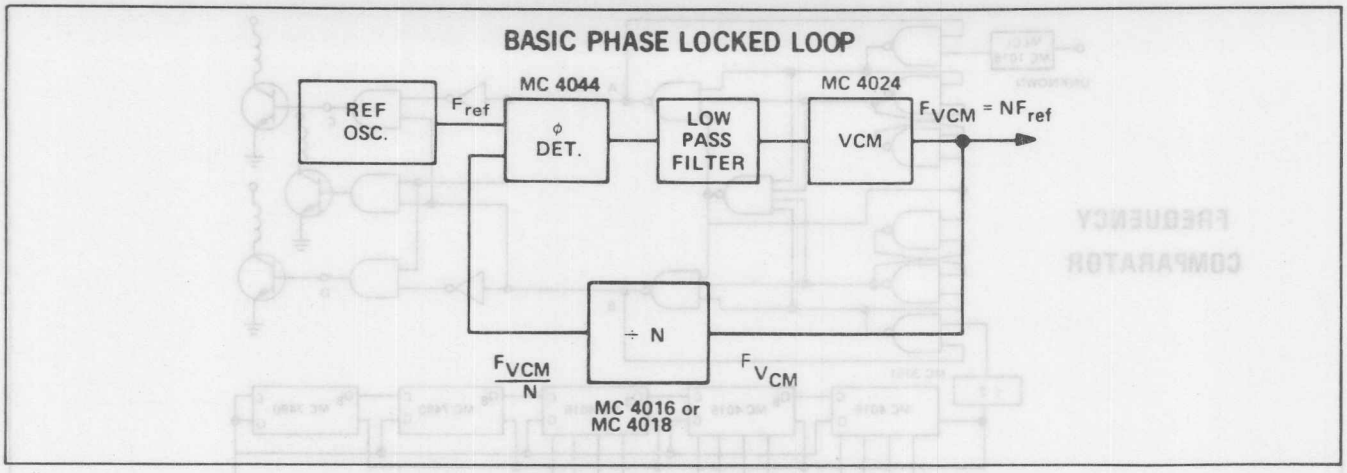


FIGURE 25

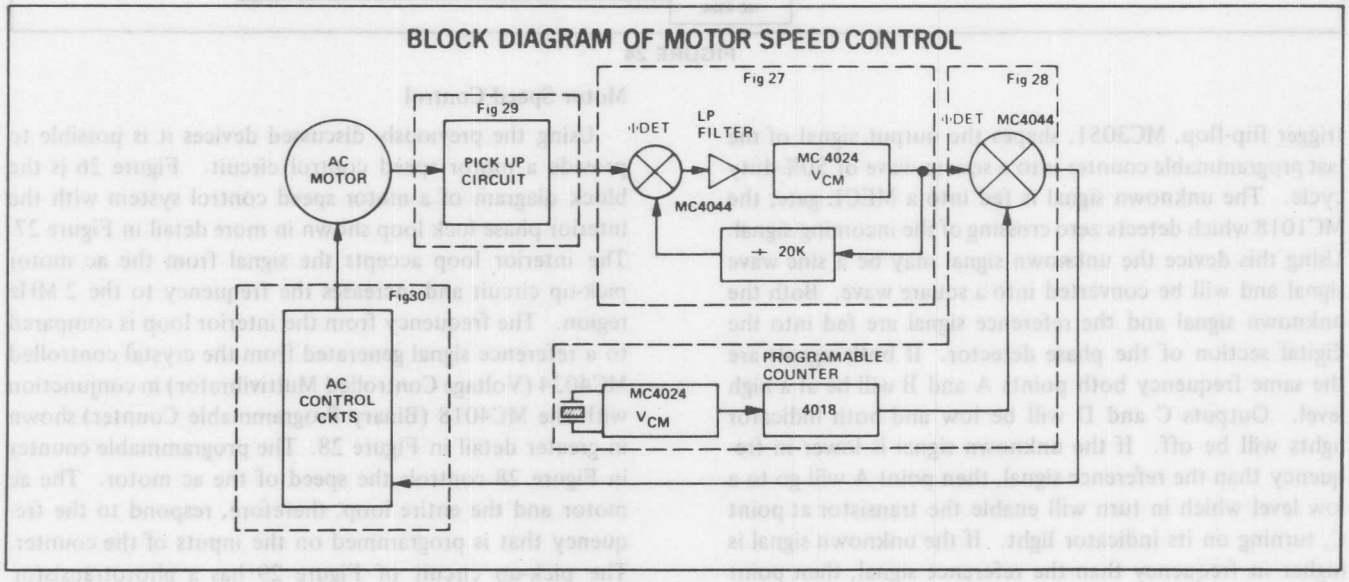


FIGURE 26

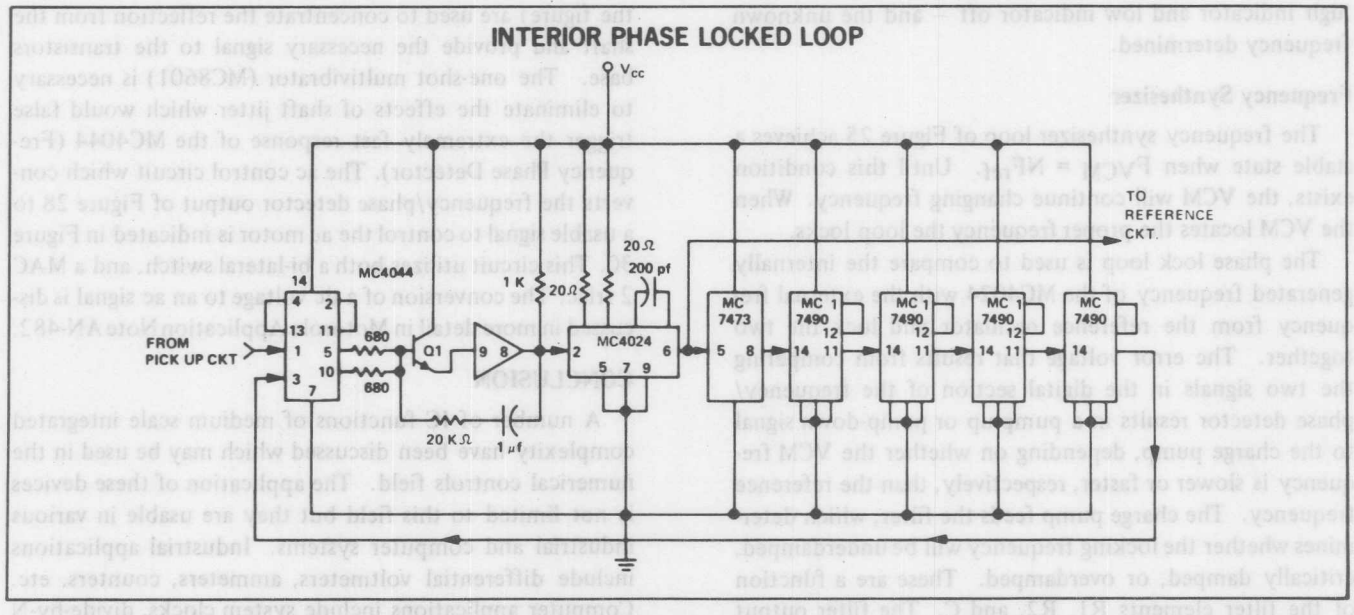


FIGURE 27

FIGURE 28

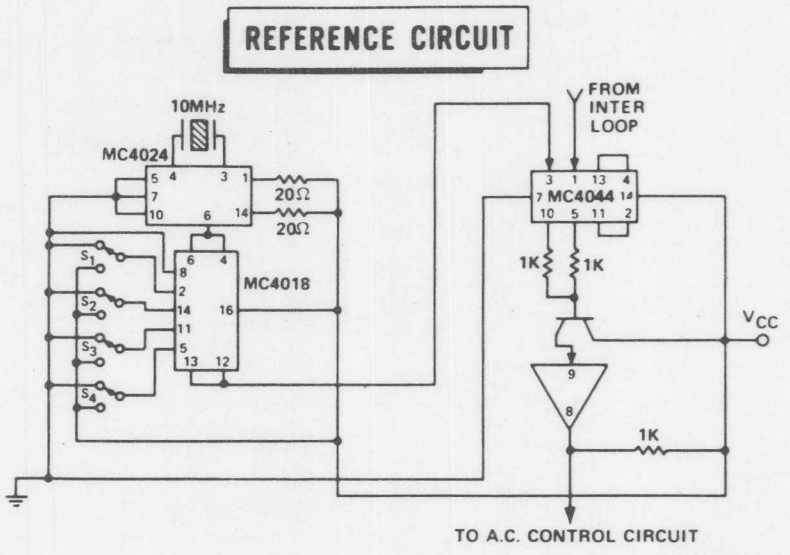


FIGURE 29

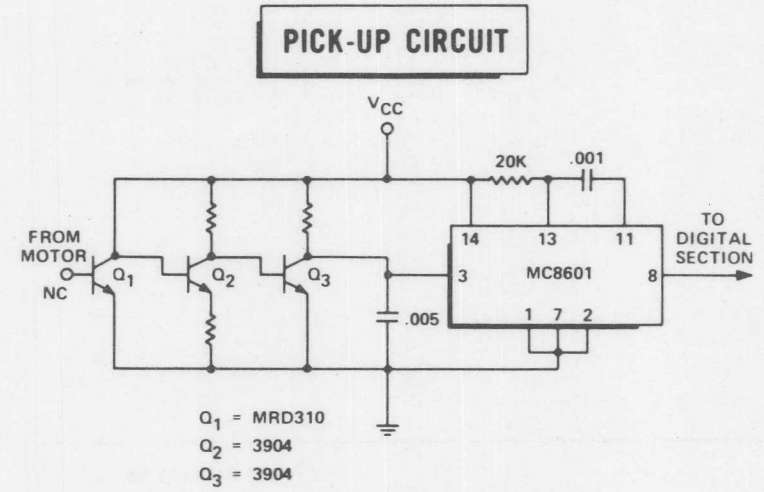


FIGURE 30